Amendments to the Specification:

Please replace paragraph 1 beginning at line 3 with the following rewritten paragraph:

--An invention for increasing wafer throughput through implementing an *in-situ* two-step etch process, is disclosed. Preferably, the *in-situ* two-step etch processes is used to etch a nitride (i.e., silicon nitride) spacer layer formed over a semiconductor substrate having a plurality of gate structures. During the first stage, an interferometry endpoint (IEP) system is implemented to detect the etch endpoint during a main etch process. Subsequently, an overetch process is performed. Preferably, the main etch process removes an etch depth of the nitride spacer layer leaving a thin layer of nitride. Thereafter, the remaining thin layer of nitride is removed in an overetch process. In one example, the etch depth is measured by implementing a distance between adjacent maximum or minimum fringes of a particular endpoint detection wavelength. In one embodiment, the thin layer of nitride is removed in the overetch process implementing the timed-etch method. In another example, [[is]] the timed-etch overetch process can be monitored by optical emission spectroscopy (OES) implementing a highly selective etch chemistry.--

Please replace paragraph 11 beginning at line 17 of page 14 and continuing to line 5 of page 15 with the following rewritten paragraph:

--Figure 5A depicts the formation of spacers 108c along sidewalls of the gates 106 subsequent to an overetch process (i.e., the second etch operation) directed toward removing a substantially thin layer 108', in accordance with one embodiment of the present invention. In one example, the overetch process is a time mode etch operation. In another example, the overetch process implementing the time mode etch method can be monitored with OES. During this etching operation, the thin layer of spacer layer 108' (i.e., over etch layer) 108' is removed implementing an etch chemistry having a substantially high selectivity __. As used herein, high selectivity is defined as the high rate of removal of the spacer layer 108' versus

the removal rate of the underlying material (e.g., oxide). In one exemplary implementation, as shown in the embodiment of Figure 5A, a portion of the underlying gate oxide layer 104 is also removed during the overetch operation despite the high selectivity of the etchant chemistry toward polysilicon and oxide. As a result, subsequent to the overetch operation, a gate oxide layer 104' having a thickness less than the gate oxide layer 104 will remain.--